SESSION 6 – TAPA II
Oversampling Converters

Thursday, June 17, 3:25 p.m.
Chairpersons: K. Nakamura, Analog Devices
S-H Lee, Sogang University

6.1 — 3:25 p.m.
A Calibration-Free 3V 16b 500kS/s 6mW 0.5mm² ADC with 0.13µm CMOS, H.-C. Choi, S.-B. You, H.-Y. Lee, H.-J. Park and J.-W. Kim, Samsung Electronics Co., Ltd., Gyeonggi-Do, Korea

A calibration-free 3V 6mW 16-bit 500kS/s cyclic ADC with an active die area of 0.5mm² is implemented in a 0.13µm CMOS. The proposed converter adopts a2.5-bit/stage cyclic architecture and capacitor layout scheme to achieve improved matching accuracy, the DNL and INL of 0.90 LSB and 6.1 LSB, respectively.

6.2 — 3:50 p.m.
A Third-order ΣΔ Modulator in 0.18µm CMOS with Calibrated Mixed-Mode Integrators, J.H. Shim and B. Kim, Korea Advanced Institute of Science and Technology, Daejeon, R.O. Korea

A third-order sigma-delta modulator employing mixed-mode integrators has been designed and implemented in 0.18um CMOS process. Because the use of mixed-mode integrators allows a 12dB improvement in the dynamic range over conventional third-order architectures, the modulator can be driven with lower sampling frequency to achieve the same dynamic range. The modulator covers the dynamic range requirements of GSM and WCDMA applications with sampling frequencies of only 3.2MHz and 40MHz, respectively. The circuit occupies 0.7mm2 silicon area.

6.3 — 4:15 p.m.
A 12 bit Continuous-Time ΣΔ Modulator with 400MHz Clock and Low Jitter Sensitivity in 0.13µm CMOS, S. Patón, A. Di Giandomenico*, L. Hernández, A. Wiesbauer*, T. Pötscher* and M. Clara*, Universidad Carlos III, Madrid, Spain, *Infineon Technologies Design Centers, Villach, Austria

A wide bandwidth Continuous-Time SIgma-Delta lowpass ADC with a 4-bit internal quantizer is presented. The converter is implemented in a pure digital 0.13um CMOS. It achieves 76dB Dynamic Range over 12MHz signal bandwidth tolerating upto 20ps RMS clock jitter. Operated at 400MHz the power consumption is 70mW from a 1.5V supply. The ADC has been designed to be tolerant to excess-loop delay and clock jitter. The 4th-order loop-filter is based on Op Amp-RC structure.

6.4 — 4:40 p.m.
A 3.3-V 240-MS/s CMOS Bandpass ΣΔ Modulator Using a Fast-Settling Double-Sampling SC Filter, V. Cheung and H.C. Luong, The Hong Kong University of Science and Technology, Kowloon, Hong Kong

A bandpass sigma-delta modulator is demonstrated to operate at a very high sampling rate of 240 MS/s by employing a proposed double-sampling switched-capacitor biquadratic filter architecture, which processes with a fast-settling feature. Implemented in a standard 0.35-um CMOS process, the modulator achieves a peak SNDR of 72 dB, 55 dB and 52 dB at a bandwidth of 200kHz, 1 MHz and 1.25 MHz for GSM, Bluetooth and CDMA2000 applications respectively while dissipating 37 mW and occupying a chip area of 1.2 mm2.

6.5 — 5:05 p.m.
An 8MHz, 72dB SFDR Asynchronous Sigma-Delta Modulator with 1.5mW Power Dissipation, S. Ouzounov, E. Roza*, H. Hegt, G. van der Weide* and A. van Roermund, Eindhoven University of Technology, Eindhoven, The Netherlands, *Philips Research Laboratories, Eindhoven The Netherlands

An Asynchronous Sigma-Delta Modulator (ASDM) that achieves a SFDR of 72 dB with a bandwidth of 8 MHz is presented. The ASDM operates as a closed-loop, nonlinear system. Spectral analysis of the ASDM shows that a center frequencyof at least 100 MHz is required for these specifications. Circuit implementations are presented and a prototype ASDM is realized in a digital 0.18 micrometer, 1.8V CMOS technology. The ASDM dissipates 1.5mW and has an area of 0.026mm2.